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Article

Capacitance Meter for Deep-level Transient Spectroscopy

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Deep-level transient spectroscopy (DLTS) is an experimental tool for studying electrically active defects in semiconductors. DLTS allows researchers to define defect parameters and measure the concentration of those defects in space charge region of simple electronic devices, typically Schottky diodes or p-n junctions. DLTS was pioneered by David Vern Lang of Bell Laboratories in 1974 and patented by him in 1975. It has a higher sensitivity than almost any other semiconductor diagnostic technique available.

DLTS involves analysis of junction capacitance versus time following a bias pulse. There are four basic devices in a DLTS measurement system: capacitance meter, a bias pulse generator, a digitizer and a computer.

The bias supply provides a bias voltage across the device under test (DUT), which is adjustable in both amplitude and duration. It's also preferable that the system offer control of the pulse transition time (rise and fall time). The range of bias voltage and pulse period varies by application. Voltages are as low as 2 volts and pulse periods are often shorter than 25 µs.

Because DLTS can detect defects at extremely low concentrations (1 part in 10^{12} of the host material's atoms) and is comparatively simple it its design, it is very popular in research labs and fields that work with unique materials. It is finding application in a wide number of industries.

Role of the Capacitance Meter

The capacitance meter presents a calibrated, real-time reference voltage proportional to the capacitance of the semiconductor under test. It provides an analog output, which can be converted to digital for further analysis using a digitizer or ADC in the test setup. Many types of instruments can fulfill this role, from a simple PC data acquisition card to a Digital Storage Oscilloscope (DSO). Boonton's model 7200 capacitance meter is well suited to DLTS applications and has been used in the following recently completed research.

Hadia Noor *et al* examined the influence of background free-carrier concentration, [*Nd* intrinsic: 10^{14} – 10^{17} cm^{-3}] induced field on the emission rate signatures of an electron point defect in ZnO Schottky devices, and determined that the Poole–Frenkel model based on Coulomb potential was found consistent. Based on these investigations, the electron trap was attributed to Zn-related charged impurity. Qualitative measurements like current-voltage and capacitance-voltage measurements were also performed to support the results. Titled "Influence of background concentration induced field on the emission rate signatures of an electron trap in zinc oxide Schottky devices," the study was originally published in the JOURNAL OF APPLIED PHYSICS, (107), 10, 103717, 2010.

"Electrical Characterization of Defects in Schottky Au–CdTe:Ga Diodes" employed a Boonton Model 7200 capacitance meter in DLTS to study deep electron states in gallium-doped CdTe using Schottky Au–CdTe diodes. Rectifying properties of diodes have been examined at room temperature current–voltage and capacitance–voltage measurements. Deep-level transient spectroscopy measurements performed in the range of temperatures 77–350 K yielded the presence of three electron traps. The thermal activation energies and apparent capture cross-sections have been determined from related Arrhenius plots. The dominant trap of activation energy E_2 = 0.33 eV and capture cross-section $\sigma_2 = 3 \times 10^{-15}$ cm^2 has been assigned to the Gallium-related DX center present in the CdTe material.

DLTS is also useful to improving many emerging fields that are used in the collection of solar energy. Deibel, Dyakonov and Parisi examined changes of defect characteristics induced by accelerated lifetime tests on photovoltaic solar cells. In their study "Defect Spectroscopy on Cu(In, Ga)$(S,Se)_2$-based Heterojunction Solar Cells: Role of the Damp Heat Treatment", the team applied current–voltage and capacitance and found that test device performance was reduced after prolonged damp heat treatment. The group observes the presence of defect states in the vicinity of the CdS/chalcopyrite interface. Their activation energy increases due to damp heat exposure, indicating a reduced band bending at the Cu(In,Ga)$(S,Se)_2$ surface. The Fermi-level pinning at the buffer/chalcopyrite interface, maintaining a high band bending in as-grown cells, is lifted due to the damp-heat exposure. The team also observed changes in the bulk defect spectra due to the damp-heat treatment.

For more information on Boonton's 7200 capacitance meter for DLTS, visit our web site: www.boonton.com.