APPLICATION NOTE

DID YOU KNOW ?

George Westinghouse (1846-1914) made a fortune with his invention of air breaks for railroad trains. He then used his wealth to form Westinghouse Electric Company; hired Nikola Tesla and Charles Proteus Steinmetz, shrewdly purchased the patent for the transformer, won the dispute with Thomas Edison over ac versus dc, and became a true giant in United States industry.

Errors, What Are They And How Bad Can They Be

Preamble

Modern integrated circuit (IC) operational amplifiers (Op Amps) have made quality instrumentation signal conditioning economically practical. Although accurate and stable Op Amp ICs are available for designing instrumentation products, there are errors associated with their applications. Specific topologies with internal IC errors often create application errors. Instrumentation Engineers should be aware of IC Op Amp errors and their impact on specific application topologies.

A complete error analysis for IC based instrumentation devices is beyond the scope of this application note; nonetheless, common internal errors specific to voltage feedback IC Op Amp circuits and a few guidelines for application topologies will be presented here.

IC Op Amp Errors

Figure 1 illustrates an Op Amp model used to identify those error parameters specified on data sheets. This model provides a first order approximation (FOA) of how these error parameters may affect application topologies. The "x" on parameters designates assumed equal values.

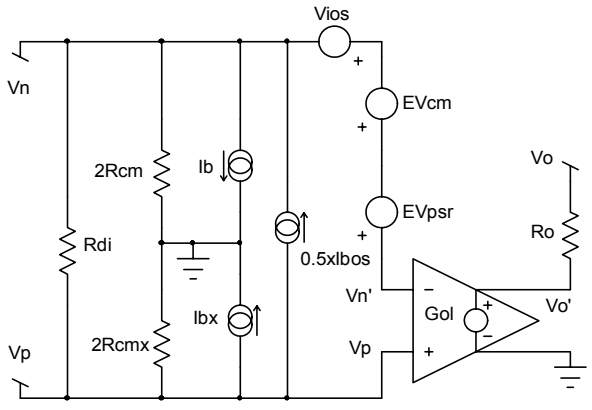

Figure 1
Op Amp Model with Error Parameters

Definitions: Reference Figure 1

1. **Rdi** is the differential input resistance between positive and negative input terminals. It is typically large enough to neglect in most practical situations; however, its value should always be examined. Data sheets specify input resistance as the resistance seen at one input with the other grounded. This data sheet parameter is Rdi in parallel with 2Rcm in Figure 1 and is essentially Rdi.

2. **Rcm** is the common mode input resistance referenced to ground as seen by a common input source connected to both positive and negative inputs. This resistance is typically in the range of hundreds of megohms and generally neglected. Data sheets seldom give this value.

3. **Ro** is the small internal output resistance as seen looking into the output terminal. In a voltage amplifier feedback topology with feedback factor "H", the effect of Ro is small (H*Ro/Gol) and is generally neglected.

4. **Ib** (bias current) and **Ibos** (offset bias current) are associated with the positive (Vp) and negative (Vn) voltage inputs, which support input currents in a "live" topology. Input currents Ip and In are specified in data sheets via parameters Ib and Ibos. Equations 1 and 2 show the definitions relating data sheet items and actual Op Amp input currents.

Ib (data sheet) ≡ [Ip + In]/2 **Eqn 1**

Ibos (data sheet) ≡ [Ip - In] **Eqn 2**

Current sources in Figure 1 support these equations.

5. **Vios** (input offset voltage) is an internal IC device voltage error (referenced to the input) that relates output voltage for zero input. IC Op Amps have internal circuits that depend on matched devices. Perfect matching can not be achieved; therefore, a mismatch voltage error term exists as Vios in Figure 1. Note that an applied voltage equal to Vios between Vn, Vp such that the voltage between Vn', Vp is zero, forces the output to zero, neglecting all other error terms.

6. **PSRR**, power supply rejection ratio, is responsible for a voltage error term referenced to the input, which relates changes in output voltage for changes in the IC supply voltages. The error term EVPSR in Figure 1 has a value of (PSRR* Δsupply voltage) for PSRRs given in data sheets as μV/V. PSRR may be given in dB for which EVpsr in Figure 1 is (Δsupply voltage * $10^{-PSRR/20}$).

7. **CMRR**, common mode rejection ratio, determines a voltage error term referenced to the input, which relates the output voltage to a common mode voltage (Vcm) applied to both positive and negative inputs. Figure 1 shows this error term referenced to the input as EVcm. Equation 3 illustrates how this error term is calculated.

$$EVcm = \frac{Vcm}{10^{CMR/20}} \qquad \textbf{Eqn 3}$$

Where; $CMR \equiv 20 * Log_{10}(CMRR)$ and where

$$CMRR \equiv \left[\frac{\text{Differential Gain}\,(G_{ol})}{\text{Common Mode Gain}\,(Gcm)}\right]$$

See Dataforth's Application Note AN103 for more detail on Common Mode issues.

Error Budget Calculations

The technique used in calculating impacts of error terms for a given application topology begins by using Figure 1 in a specific application topology and solving for the analytical output voltage (Vo) expression using Eqn 4, which neglects Ro.

$$Vo = Vo' = Gol * (Vp - Vn') \qquad \textbf{Eqn 4}$$

Where Vp is the external voltage on the positive input as determined by the application topology and Vn' is the negative external input voltage (Vn) as determined by the application topology plus the accumulated internal errors.

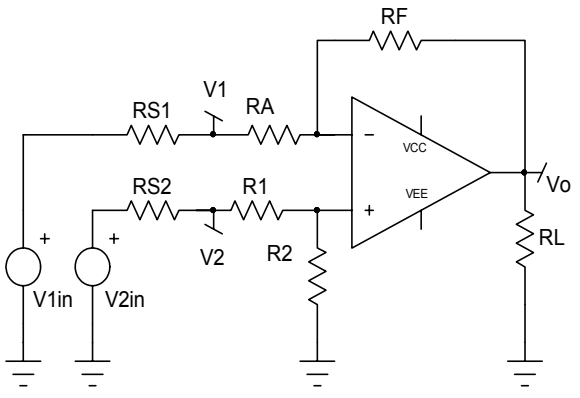

Figure 2
Single Stage Difference Amplifier

Figure 2 is the difference amplifier topology chosen for analysis in this Application Note because it is particularly vulnerable to resistor tolerances. Errors dominated by external resistor tolerances may justify a topology change; therefore, errors due to external resistors should always be examined first before internal IC errors are analyzed.

RS1 and RS2 are the source resistors for input source voltages V1in and V2in respectively. Often users forget to include these resistors when considering a specific application. When these resistors are large compared to RA and R1, they cause additional errors. Later in this Application Note, a topology will be recommended in which the impact of source resistors is diminished.

For now, assume the input voltage sources are near ideal (i.e. RS1=RS2=0). Using concepts embodied in Eqn 4, the output voltage (Vo) in Figure 2 is illustrated by Eqn 5.

$$Vo = Gp * V2 - Gn * V1 \qquad \textbf{Eqn 5}$$

Where terms Gn and Gp are the negative gain and positive gain respectively as shown;

$$Gp = [R2/(R2+R1)] * \left\{G_{ol}/[1 + G_{ol} * RA/(RF+RA)]\right\}$$

$$Gn = [RF/(RF+RA)] * \left\{G_{ol}/[1 + G_{ol} * RA/(RF+RA)]\right\}$$

The terms Rcm, Rdi, RS1, RS2, and Ro are neglected in deriving Gp and Gn in Eqn 5.

If $G_{ol} * [RA/(RF+RA)] >> 1$ and if RA=R1, RF=R2; then Eqn 5 becomes the classic difference gain equation shown in Eqn 5a.

$$Vo = (V2 - V1) * (RF/RA) \qquad \textbf{Eqn 5a}$$

It is clear that mismatches in {RA; R1} and {RF; R2}, can cause errors; moreover, Eqn 5a is less correct if, $G_{ol} * [RA/(RF+RA)]$ is not >> 1

Note: Equations 5, 5a conform to the general feedback equations; namely,
Gain closed loop =Gol/(1+Gol*H); where H is the voltage feedback factor and Gol is the amplifier open loop gain. For Gol*H>>1, Gain closed loop ≅1/H.

Gain Error due to Resistance Tolerance

Table 1 illustrates how resistor tolerances in Figure 2 impact the circuit gain for a random lot with open loop gain (Gol) constant. Note that the net percent error due to resistor tolerances alone can be very significant in this topology.

Next after examining the variations in gain due to resistor tolerance, the effects of CMMR, PSRR, Vios, Ib, and Ibos are analyzed. The following error calculations are derived with; Eqns 3,4,and 5; V1=V2=zero; Rdi, Rcm, Ro, RS1, RS2 neglected; and $G_{ol} * [RA / (RF + RA)] >> 1$. Throughout all these calculations RF=R2 and RA=R1.

Internal Offset Voltage (Vios) Error

The output voltage error caused by an Op Amp's internal mismatch voltage error term Vios is shown in Eqn 6 for the topology of Figure 2, using the Op Amp error model in Figure 1.

$$\text{Vo error} = \pm \text{Vios} * (1 + RF / RA) \qquad \textbf{Eqn 6}$$

The Vios term is always shown in data sheets as a positive value; however, it is randomly either negative or positive.

Input Current Error

Input currents Ip and In on both the positive and negative inputs flow through the DC Thevenin Resistance associated with each input and develop unwanted voltages, which are amplified by the application topology. Eqn 7 shows this error for the topology in Figure 2, using the error model in Figure 1 with Eqns 1, 2.

$$\text{Vo error} = \ldots\ldots$$
$$\left[\text{Ib} * (R_-^T - R_+^T) \pm \text{Ibos} * (R_-^T + R_+^T)/2\right] * (1 + RF / RA) \qquad \textbf{Eqn 7}$$

Note: Ib Error term is zero **IF** $R_-^T = R_+^T$ where;

$R_-^T = RF * RA / (RF + RA)$ and $R_+^T = R1 * R2 / (R2 + R1)$

Reminder:
Input Ib on data sheets is positive (into) for "n-type" devices and negative (out) for "p-type" devices; however, Ibos is always randomly either positive or negative.

CMRR Error

As previously discussed internal mismatches in the Op Amp cause output errors. Another example of this type error is the term EVcm, which is referenced to the input in Figure 1. The associated output error due to this term is shown in Eqn 8 for the topology in Figure 2.

$$\text{Vo error} = \text{Vcm}^T * (10^{-\text{CMR}/20}) * (1 + RF / RA) \qquad \textbf{Eqn 8}$$

Note: In Figure 2, one can assume that the external voltage between Op Amp inputs is essentially zero. Therefore, any Thevenin voltage on the Op Amp positive (+) input is essentially the common mode voltage (a quick trick to identifying, Vcm^T).

PSRR Error

Another error due to Op Amp internal mismatches is an output voltage change for changes in the power supply voltages. Figure 1 shows this error term referenced to the input as EVpsr. Equation 9 is the output error voltage for an Op Amp PSRR given in data sheets as µV/V.

$$\text{Vo error} = (\text{PSRR} * \Delta \text{supply volts}) * (1 + RF / RA) \qquad \textbf{Eqn 9}$$

When PSRR is given in dB, Eqn 9 becomes;

$$\text{Vo error} = \left[(\Delta \text{supply volts}) * \left(10^{-\text{PSRR}/20}\right)\right] * (1 + RF / RA)$$

Example of Typical Error Calculations

Typical Op Amp values for the difference amplifier topology of Figure 2 at 25° C is shown below. Change in power supply voltage is assumed to be 500mV.

Rdi = 800 kΩ	Rcm = 65 MΩ	RF = 200 kΩ
RA = 5kΩ	R2 = 200kΩ	R1 = 5kΩ
Ibos = 200 nA	Vios = 5 mV	Ib = 500 nA
IbosTC = 1nA/°C	ViosTC= 5µV/°C	Ib TC =No Value
PSRR = 20 µV/V	CMRR = 90 dB	Gol= 50k-200k
RS1 = 10 Ω	RS2 = 10 Ω	Vcm^T = 15 volts

Individual error calculations

Most parameters have temperature coefficients (TC), which should be examined. The following calculations use only the TC values for Vios, and Ibos. The temperature multiplier is TC*(Ta −25°C). The term (Ta) is ambient temperature and limited to 40°C.

In this example, input referenced error terms are multiplied by the closed loop gain, which is given as $[G_{ol} / [1 + G_{ol} * RA / (RF + RA)]$ and reduces to; 41 for $G_{ol} = \infty$; 40.97 for $G_{ol} = 50k$; and 40.99 for $G_{ol} = 200k$.

- **Vios Error** = [5mV+5µV/*(40-25)]*41 = **208.08 mV**
- **Ib Error = Zero**, since $R_-^T = R_+^T$ if RF=R2; RA=R1
- **Ibos Error** =[200nA+1nA/°C* (40-25)]*4.88k*41=**43mV**
- **CMRR Error** = 15V* $10^{-90/20}$ *41 = **19.45mV**
- **PSRR Error** = 20µV/V*500mV*41 =**410µV**
- **Total Error** ≅ (on the order of) **271 mV**.

These calculations are not precise; nonetheless, this approach predicts error magnitudes and illustrates the most dominant parameter, Vios in this case. Clearly this particular configuration is not suitable for low-level dc measurements; for example, measuring current with a 100 ampere, 50mV resistance shunt (500µΩ)

Table 2 illustrates how error parameters in Figure 1 impact the total output voltage for the difference amplifier in Figure 2.

Single Stage Difference Amplifier Observations

The above analysis of Figures 1,2 shows;
1. Resistor tolerances do cause serious errors.
2. Thevenin resistance at each (±) input should be equal
3. Avoid high Vcm voltages.
4. Input source resistors RS1, RS2 should be zero or RS1 much less than RA and RS2 much less than R1.
5. Op Amp open loop gains (Gol) should be very high.
6. Avoid large ambient temperature swings.

The Instrument Amplifier

Figure 3 illustrates the basic instrumentation amplifier topology. In general, all individual internal Op Amps are fabricated on a single die or substrate and matched within the fabrication process capabilities. Resistors RF1, RF2 are internally fabricated on the die and matched. Resistor RG is usually external and controls the amplifier gain.

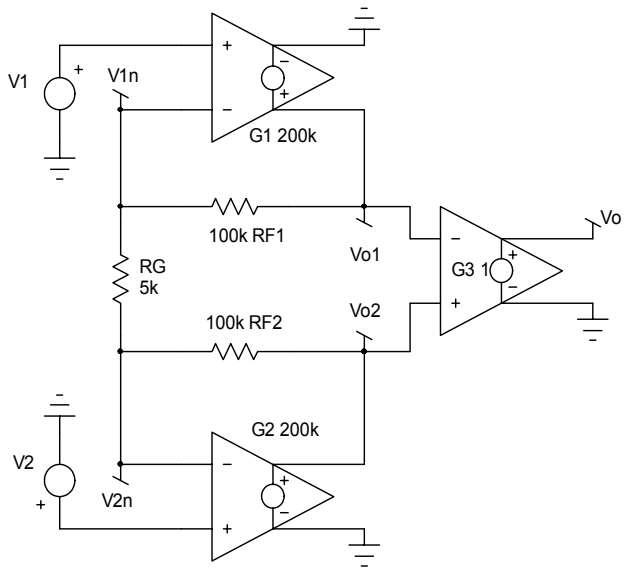

Figure 3
Basic Instrumentation Amplifier Topology

In calculating the overall gain for this topology, amplifiers G1, G2, are assumed to be near ideal with G3 an ideal unity gain amplifier. Specifically Ro, Rdi, Rcm, and error parameters in Figure 1 are neglected. The output stage G3 is typically the difference amplifier of Figure 2.

Equation 10 is the ideal expression for output voltage.

$$Vout = (V_{o2} - V_{o1}) = (V2 - V1)*\left(\frac{2RF}{RG}+1\right) \qquad \textbf{Eqn 10}$$

It is interesting to examine the effects Op Amp gains and non-identical RFs. This can be achieved by writing two node equations at Vn1 and Vn2, then solving for Vo1 and Vo2. Equation 11 illustrates the results.

Vout = (Vo2-Vo1) =

$$\frac{V2*\left[\frac{RF_1+RF_2}{RG}+1\right]*\left[\frac{G_1+1}{G_1}\right] - V1*\left[\frac{RF_1+RF_2}{RG}+1\right]*\left[\frac{G_2+1}{G_2}\right]}{1+\left[\frac{RF_2}{RG}+1\right]*\frac{1}{G_2}+\left[\frac{RF_1}{RG}+1\right]*\frac{1}{G_1}+\left[\frac{RF_1+RF_2}{RG}+1\right]*\left[\frac{1}{G_1*G_2}\right]} \qquad \textbf{Eqn 11}$$

Although the gains (G_1,G_2) may not be equal, they can be assumed very large numbers and, therefore, set to a single very large gain (G) in Equation 11. In addition, if this gain (G) is >>> than [(RF1+RF2)/RG +1], then Equation 11 becomes;

$$Vout = (V_{o2} - V_{o1}) = (V2 - V1)*\left(\frac{RF_1+RF_2}{RG}+1\right) \qquad \textbf{Eqn 12}$$

Note: The single resistor (RG) is responsible for changing gains of an Instrument Amplifier since RFs are internally fixed in the die. Moreover, the matching of RFs is usually so close that Equation 10 is valid. Furthermore, if the TC of RG and RF match, then the instrument amplifier gain expression is essentially independent of temperature.

Table 3 illustrates how random values of gain and resistor values can impact the instrumentation amplifier net gain.

The error parameters of the Op Amp shown in Figure 1 cause output errors in an Instrument Amplifier. Errors are analyzed here to obtain first order approximation (FOA) insight into how they impact the output. The analytical process begins by substituting the model of Figure 1 for the amplifiers G1 and G2 in Figure 3.

Some reasonable assumptions are made to ease the math burden but not mask the dominant impact caused by error parameters.

These assumptions are;
(a) neglect Rdi, Rcm, and PSRR,
(b) resistors RP1, RP2 (source resistors of V1in and V2in) exist in the two input lines,
(c) Ip1, Ip2 are the two input currents and assumed equal to Ip (illustrates the effects of Rp1 ≠ Rp2),
(d) CMRR1 ≠ CMRR2; Vios1 ≠ Vios2; Ibn1 ≠ Ibn2,
(e) RF1 = RF2; G1 = G2 = G,
(f) Inputs V1 and V2 are the common mode voltages (Vcm) on amplifiers G1 and G2 in Figure 3, and
(g) G3 in Figure 3 is an ideal unity gain amplifier.

Instrument amplifier major errors are due to external topology and the front-end Op Amp cells G1 and G2. The error equations shown below neglect non-zero errors in G3 (difference cell). These equations are presented to illustrate the impact of external application topologies.

These assumptions predict (Vo2-Vo1) errors as follows;

$$\text{Vios Error} = (\text{Vios1} - \text{Vios2}) * \left(\frac{2\text{RF}}{\text{RG}} + 1\right) \quad \textbf{Eqn 13}$$

$$\text{Ip Error} = (\text{Rp1} - \text{Rp2}) * \text{Ip} * \left(\frac{2\text{RF}}{\text{RG}} + 1\right) \quad \textbf{Eqn 14}$$

$$\text{In Error} = (\text{In2} - \text{In1}) * \text{RF} \quad \textbf{Eqn 15}$$

$$\text{CMR Error} = \left(\text{V1} * 10^{-\text{CMR1}/20} - \text{V2} * 10^{-\text{CMR2}/20}\right) * \left(\frac{2\text{RF}}{\text{RG}} + 1\right) \quad \textbf{Eqn 16}$$

Note: Instrument Amplifier CMR is specified in data sheets as a net quantity, which includes the effect of all internal gain cells.

Table 3 illustrates the impact of error parameters on the output voltage of the instrument amplifier in Figure 3.

Premium IC instrumentation amplifiers have well matched front-end Op Amps (G1,G2); consequently, Eqns 13 and 15 reduce to near zero. Moreover, if the engineer ensures an application, which has Rp1=Rp2, then Eqn 14 reduces to near zero. Instrumentation amplifiers with high CMR in cells G1,G2, and G3 minimize the impact of Eqn 16.

Clearly the Instrumentation Amplifier is a superior conditioning and instrumentation front-end topology compared to the single stage difference topology. Unfortunately, instrumentation amplifiers are not completely error free. Manufactures of Integrated Circuit (IC) Instrumentation Amplifiers do specify in their data sheets a set of net "error" terms, which apply to the total IC amplifier. For example; Vios, CMR, Ib, Ibos, Rinputs, etc are all specified as net device terms.

DATAFORTH MEASUREMENT DEVICES

Integrated circuit operational amplifier internal error terms do cause circuit topology dependent errors. Dataforth design engineers are imminently aware of these phenomena and use every available technique to minimize the impact of these error components on Dataforth's products. For example, Dataforth uses only premium IC's in their design together with unique patented circuit topologies to minimize errors. Moreover, all Dataforth modules are thoroughly tested and subjected to a thermal burn-in. In addition, internal voltage offset errors and gain errors due to resistor tolerance are removed by individual tuning on each module. Consequently, Dataforth has developed a quality cost effective product line of signal conditioning modules. The reader is encouraged to visit Dataforth's website www.Dataforth.com for detail information on all Dataforth's product The following are just a few of Dataforth's outstanding module benefits;

- Dataforth signal conditioners use high performance amplifiers internally, which have low offset voltages (Vos) and low Vos TC. Residual errors due to Vos internal errors are calibrated out prior to shipment.
- Zero and Span errors caused by internal resistor tolerances are calibrated out prior to shipment. High performance amplifiers and discrete components ensure low drift over the wide operating range of -40C to +85C. Dataforth's amplifiers and associated adjustment networks provide stable calibration; therefore, after the modules are sealed no periodic calibrations are required.
- All Dataforth circuitry is designed to be insensitive to variations in power supply voltage. SCM5B modules operate over 4.75V to 5.25V with a power supply rejection (PSR) as low as 2uV per % variation in supply voltage, referred to input. SCM7B and DSCA modules operate over a much wider supply voltage range of 14 to 35V with PSR as low as 0.0001% of output per % variation in supply voltage.
- High input impedances (50 Meg ohms for 5B30-xx modules and 200 Meg ohms for 5B40-xx modules) allow interfacing to sensors with high output impedance. The use of FET input amplifiers result in low bias currents of 0.5nA, benefiting the user in allowing interfacing to sensors with high output impedance.
- Dataforth's patented unique iso-chopper isolation barrier allows continuous input common mode signal levels up to 1500Vrms (2200V peak). Common Mode Rejection of up to 160dB ensures signal integrity in extreme applications.

As an example consider measuring steady-state line current of a three-phase 3-wire delta connected AC motor using Dataforth's SCM5B40/41 wide bandwidth analog voltage module and a four-wire shunt sensor. Figure 4 illustrates the modular structure of Dataforth's SCM5B40/41 used in this example. Three phase line current shunt measurements on delta 3-wire devices must be done with low voltage (typically 50mV) shunts to maintain balanced load conditions. Such low voltage measurements require accurate modules, which must maintain accuracy at common mode voltages equal to AC line values.

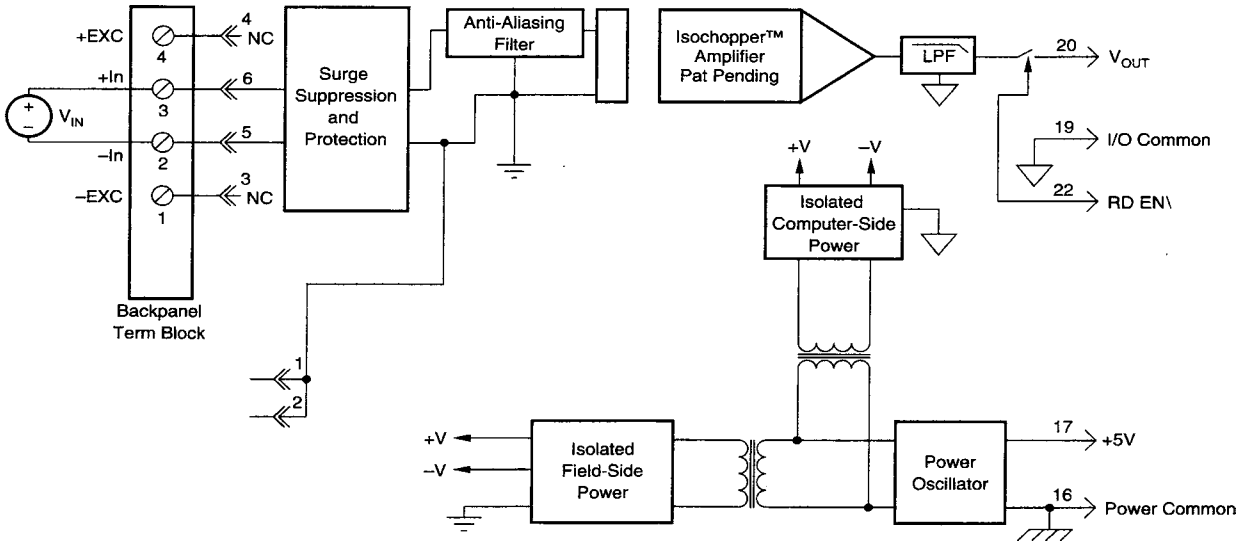

Figure 4
Dataforth SCM5B40/41 Isolated Analog Module

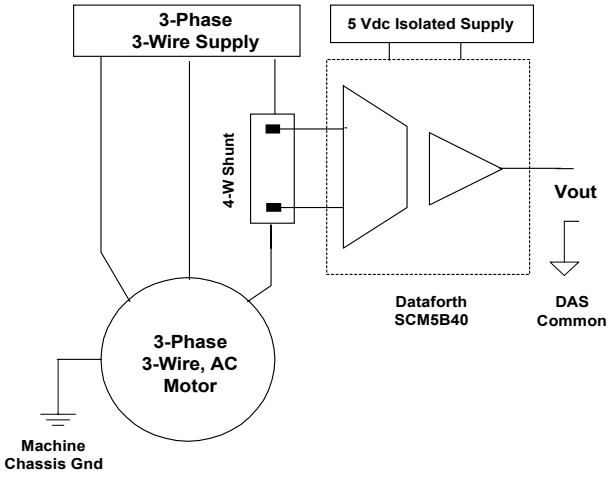

Figure 5
3-Phase Line Current Measurement

Figure 5 illustrates a line current measurement for a 100 horsepower 3-phase 460 volts AC (126 A rms full load), 60 Hz delta connected motor. Dataforth's SCM5B40-02 module (output –5 to +5 volts, input –50mV to +50mV, gain 100V/V) is used to sense line current in a 300A, 50mV, 166.667μΩ shunt. Shown below are error calculations using Dataforth's specifications. See Dataforth's AN104 for more specification details.

- **Input Resistance:** 200MΩ ,40kΩ off/overload This has insignificant effect on the net R_{shunt} resistance.
- **CMV:** 100 dB (1500Vrms input/output max). Common mode voltage input/output is 267 (462÷√3) Vrms, for this balanced motor with negligible IR drops in the building ground structure. The error is $267V*10^{(-100/20)}$ = 2.67 mV rms See AN103 on CMR.
- **Power Supply Sensitivity:** 2μV/% RTI. The error is ±2μV/%*5%*100V/V = ± 1mV rms, for a 5% variation in the 5 volt module power supply..
- **Input Bias Current:** ±0.5nA. The error is ±0.5nA*R_{shunt}*100V/V, certainly negligible.
- **Accuracy:** Includes nonlinearly, hystersis, and repeatability; (a) ±0.05% of Span; (b) ±10μV RTI; (c) ±0.05% of V_z. Errors are determined as follows;
  a) (±0.05%)*10V = ± 5mV rms ,
  b) (±10μV)*100 V/V = ± 1mV rms ,
  c) (±0.05%)*0mV =± 0 V rms (Vz =0 V)
- **Stability:** Input offset ±1μV/°C; Output offset ±40μV/°C; Gain ±25 ppm/°C of reading. For a temperature of 122°F, (25°C change from 25°C room), stability calculations in volts rms are;
  * Input offset ±1μV/°C*25°C*100 V/V= ± 2.5mV
  * Output offset ±40μV/°C*25° = ± 1mV.
  * Gain 25μV/°C*25°C*5 = ± 3.1 mV, max.

Random (±) terms will likely not be the same sign; hence, adding would give an unlikely net error. Another method for adding ± random mutually exclusive rms values is the square root of the sum of squares of each (±) term. This method gives an estimated net error of ± 7.14mV rms.
Note A 10 mV error represents only a 0.6 ampere error.

Table 1

Single Stage Op Amp Difference Amplifier Gain Error
Reference Figure 2

Table 1 is available on Sheet #1 of the interactive Excel Workbook from Dataforth's Web site. The reader is encouraged to download this Excel file http://www.dataforth.com/catalog/pdf/an102.xls , choose their own values, follow instructions, and examine the effects of their own selected resistor, gain, temperature, and tolerance values.

								Nominal Values		
R%	Gol	RFo	RAo	R1o	R2o	V1-	V2 +	Gn-	Gp+	Vout
5	2.0E+05	2.0E+05	5000	5000	2.0E+05	1.20	1.10	39.992	39.992	-3.999

			Gn-				Gp+	Actual	Output	
RF	RA	Gn-	% Error	R1	R2	Gp+	% Error	Vout	% Error	% Error
209898	5188	40.45	1.15	4892	201175	40.47	1.19	-4.03	0.72	**Max**
192146	4944	38.87	-2.81	5007	204481	38.91	-2.71	-3.84	-3.89	7.48
192585	4998	38.53	-3.66	5147	193480	38.50	-3.74	-3.89	-2.78	**Min**
209156	5227	40.02	0.06	5219	199629	39.96	-0.07	-4.06	1.53	-6.88
206009	4996	41.23	3.11	5208	206813	41.19	2.99	-4.17	4.38	
203990	5036	40.50	1.28	4907	201595	40.51	1.29	-4.04	1.13	
205909	5186	39.71	-0.71	4834	206645	39.77	-0.56	-3.90	-2.41	
203815	4893	41.65	4.15	4845	204523	41.65	4.16	-4.16	4.04	
194064	4863	39.90	-0.22	5111	193484	39.84	-0.37	-4.06	1.45	
202765	5079	39.92	-0.17	4875	192133	39.90	-0.22	-4.02	0.40	
192751	4803	40.13	0.35	4757	200604	40.17	0.45	-3.97	-0.71	
194706	5000	38.94	-2.63	4788	206005	39.03	-2.42	-3.80	-4.97	
196937	4854	40.57	1.45	4862	193200	40.54	1.38	-4.09	2.25	
209832	5225	40.16	0.41	5151	200225	40.12	0.31	-4.06	1.53	
198148	4989	39.72	-0.69	4963	207961	39.76	-0.58	-3.92	-1.87	
203014	4792	42.36	5.92	4862	196456	42.30	5.78	-4.30	7.48	
205060	5055	40.56	1.43	4772	192139	40.55	1.39	-4.07	1.86	
201209	5201	38.69	-3.27	4897	190500	38.68	-3.27	-3.87	-3.20	
199252	4923	40.48	1.21	5212	205734	40.44	1.13	-4.08	2.12	
206517	4968	41.57	3.94	4788	203140	41.58	3.96	-4.14	3.63	
198588	5249	37.83	-5.40	5173	208742	37.88	-5.27	-3.72	-6.88	
206699	5182	39.89	-0.26	4852	207714	39.95	-0.11	-3.92	-1.87	
202608	5116	39.60	-0.97	5106	190928	39.54	-1.14	-4.03	0.83	
209891	4987	42.09	5.25	4939	199391	42.04	5.12	-4.26	6.64	
196508	5099	38.54	-3.64	5034	204021	38.58	-3.53	-3.81	-4.74	
206259	5219	39.52	-1.17	5183	207945	39.53	-1.16	-3.95	-1.35	
203276	4920	41.32	3.31	5155	190426	41.19	3.00	-4.27	6.73	

Table 2

Single Stage Op Amp Difference Amplifier Error Budget [1]
Reference Figure 1

Table 2 is available on Sheet #2 of the interactive Excel Workbook from Dataforth's Web site. The reader is encouraged to download this Excel file http://www.dataforth.com/catalog/pdf/an102.xls , choose their own values, follow instructions, and examine the effects of their own selected values.

Temp C°	VcmT	Res %	RFo	RAo	R2o	R1o	CMR-db
40	5	5	2.00E+05	5.00E+03	2.00E+05	5.00E+03	90

Random Total	
Error Max	Error Min
1.29E+00	-1.18E+00

			Manufacture's Variation					
Ib	Ibos	Vios	Ib%	%Ibos	%Vios	Ib TC	Ibos TC	Vios TC
5.00E-07	2.00E-07	5.00E-03	30	30	50	3.00E-09	1.00E-09	1.00E-03
	(T-25)*TC							
4.50E-08	1.50E-08	1.50E-02						

RF	RA	R2	R1	Ib	Ibos	Vios	Ib Error Vout	Ibos Error Vout	Vios Error Vout	CMR Error Vout	Total Error Vout
193102	5038	206774	4989	4.83E-07	1.93E-07	-1.97E-02	7.32E-04	3.76E-02	-7.77E-01	6.22E-03	-7.32E-01
191335	5153	195247	4830	5.55E-07	2.10E-07	1.99E-02	6.44E-03	3.94E-02	7.60E-01	6.03E-03	8.12E-01
205315	4808	193496	4908	5.67E-07	2.48E-07	-1.87E-02	-2.21E-03	5.20E-02	-8.19E-01	6.91E-03	-7.63E-01
205654	5117	207763	4798	6.28E-07	-1.88E-07	2.20E-02	7.82E-03	-3.79E-02	9.06E-01	6.51E-03	8.82E-01
191690	4861	203498	5218	5.80E-07	2.38E-07	1.91E-02	-8.14E-03	4.79E-02	7.72E-01	6.39E-03	8.19E-01
204455	5249	204525	4962	6.86E-07	1.74E-07	-1.78E-02	7.49E-03	3.51E-02	-7.11E-01	6.32E-03	-6.63E-01
191123	4893	196013	5084	5.50E-07	-1.74E-07	-2.16E-02	-4.08E-03	-3.44E-02	-8.67E-01	6.33E-03	-8.99E-01
194164	4903	200494	5214	5.26E-07	2.69E-07	2.08E-02	-6.40E-03	5.47E-02	8.45E-01	6.42E-03	8.99E-01
198688	4795	191002	5071	6.45E-07	-2.51E-07	-1.94E-02	-7.07E-03	-5.20E-02	-8.24E-01	6.71E-03	-8.76E-01
190055	5050	203453	4765	4.37E-07	-2.71E-07	2.05E-02	4.45E-03	-5.06E-02	7.92E-01	6.11E-03	7.52E-01
199956	5233	207930	4819	4.44E-07	-2.73E-07	-2.16E-02	6.78E-03	-5.31E-02	-8.48E-01	6.20E-03	-8.89E-01
193480	4864	198482	5069	4.50E-07	-2.56E-07	1.94E-02	-3.63E-03	-5.12E-02	7.90E-01	6.45E-03	7.42E-01
202350	4950	193810	5083	4.48E-07	2.74E-07	2.05E-02	-2.28E-03	5.68E-02	8.57E-01	6.62E-03	9.18E-01
204159	4831	203058	5213	6.18E-07	1.85E-07	-2.05E-02	-9.71E-03	3.98E-02	-8.86E-01	6.84E-03	-8.49E-01
209620	4889	194672	5121	4.69E-07	2.43E-07	-1.88E-02	-4.36E-03	5.28E-02	-8.27E-01	6.94E-03	-7.71E-01
198405	5243	206783	5187	6.84E-07	-1.91E-07	-2.24E-02	1.27E-03	-3.83E-02	-8.70E-01	6.14E-03	-9.01E-01
195662	5221	192646	4898	4.43E-07	-2.71E-07	1.85E-02	5.26E-03	-5.21E-02	7.12E-01	6.08E-03	6.71E-01
202552	4912	203547	5165	4.82E-07	2.38E-07	2.24E-02	-4.92E-03	5.01E-02	9.45E-01	6.68E-03	9.97E-01
206336	4998	196925	4917	6.59E-07	1.62E-07	-2.02E-02	2.32E-03	3.35E-02	-8.52E-01	6.69E-03	-8.10E-01
205725	4821	197022	4800	5.44E-07	-1.79E-07	-2.24E-02	5.83E-04	-3.72E-02	-9.77E-01	6.91E-03	-1.01E+00
201991	5003	192550	4836	4.14E-07	2.69E-07	1.94E-02	2.83E-03	5.40E-02	8.02E-01	6.54E-03	8.66E-01
191320	4781	207967	5020	6.53E-07	-2.33E-07	1.85E-02	-6.35E-03	-4.64E-02	7.60E-01	6.48E-03	7.14E-01

Note:

1 Gol*RA/(RA+RF) Assumed >>>1 with Ro, Rdi, Rcm, PSRR neglected

Table 3

Instrument Amplifier Error in Gain (2RF/RG+1) Including Error Parameter Analysis [1]
Reference Figure 3

Table 3 is available on Sheet #3 of the interactive Excel Workbook from Dataforth's Web site. The reader is encouraged to download this Excel file http://www.dataforth.com/catalog/pdf/an102.xls , choose their own values, follow instructions, and examine the effects of their own selected values

G1o	G2o	RF1o	RF2o	RGo	V1	Exact Δ_{21} Vout	Eqn 12 Δ_{21} Vout	% Error Δ_{21} Vout
2.00E+05	2.00E+05	1.00E+05	1.00E+05	5000	1.00	4.099	4.100	2.05E-02
G%	**G%**	**R%**	**R%**	**R%**	**V2**		**Gain**	
20	20	0.1	0.1	1	1.10		41	

Error Analysis for RF1o = RF2o Eqns 13,14,15,16							Errors
CMR1-db	**CMR2-db**	**Rp1**	**Rp2**	**Ip2 = Ip1**	**Δ_{21} In**	**Δ_{12} Vios**	**Δ_{21} Vout**
100	90	6.00E+03	4.00E+03	5.00E-08	2.00E-09	1.000E-03	2.58E-02
Error		**Error**			**Error**	**Error**	
-1.02E-03		4.10E-03			2.00E-04	4.10E-02	

Random Gain Error Analysis						Δ_{21} Vout	Eqn 12	Exact
G1	**G2**	**RF1**	**RF2**	**RG**	**Δ_{21} Vout**	**% Error**	**Gain**	**Gain**
203525	174864	99962	100005	5031	4.074	-6.32E-01	40.749	40.741
226311	183534	99953	100078	5030	4.076	-5.92E-01	40.766	40.757
205449	184110	99982	99958	4965	4.126	6.30E-01	41.267	41.258
160380	174330	100090	100013	4965	4.130	7.23E-01	41.305	41.296
189823	184638	100038	99986	4972	4.122	5.33E-01	41.228	41.219
229027	200575	100042	99997	4967	4.126	6.46E-01	41.274	41.265
198000	222777	99944	100077	5037	4.070	-7.23E-01	40.713	40.703
185516	173917	100097	99960	5042	4.067	-8.02E-01	40.680	40.671
180830	205588	99969	100007	5034	4.071	-7.00E-01	40.722	40.713
163181	166445	100079	100042	5032	4.076	-5.82E-01	40.770	40.761
196510	169837	100055	99930	5013	4.088	-2.82E-01	40.893	40.884
184617	234514	100029	99989	5036	4.071	-7.18E-01	40.715	40.706
204613	235265	99966	100084	5043	4.066	-8.37E-01	40.666	40.657
171270	187169	100018	100037	4959	4.133	8.01E-01	41.338	41.328
238467	172733	99916	99923	4953	4.134	8.21E-01	41.345	41.337

Note:

1 Ro, Rdi, Rcm, PSRR neglected